REMARKS

Examiner Lattin is thanked for his thorough examination of the Subject Patent Application. Reconsideration of the rejection of Claim 5 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is requested, based on the following.

Claim 5, has been cancelled, so the objection is now considered moot.

Reconsideration of the rejection of Claims 1, 3 - 5, 8, 11, 14 and 15 under 35 USC 102 (b) as being anticipated by Fisher (US 6,111,267), is requested, based on the following.

Claims 1, 3 - 5, 8, 11, 14 and 15 have been cancelled, so the rejection os now considered moot.

Reconsideration of the rejection of Claim 2 under 35 USC 103(a) as being unpatentable over Fisher (US 6,111,267) in view of Wolf, s., is requested, based on the following.

Claim 2 has been cancelled, so the rejection is now considered moot.

Reconsideration of the rejection of Claims 6, 7, 9, 10, 12 and 13 under 35 USC 103(a) as being unpatentable over Fisher (US 6, 111, 267) in view of Kudo (US 6,190,975) is requested, based on the following.

Claims 6, 7, 9, 10, 12 and 13 have been cancelled, so the rejection is now considered mot.

Allowance of all non-cancelled Claims (Claims 16 - 27),is requested.

TSMC01-1132

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached page is captioned.

"Version with markings to show changes made"

It is requested that should Examiner Lattin not find that the Claims are now Allowable that he call the undersigned attorney at 845-452-5863, to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

PLEASE AMEND THE CLAIMS AS FOLLOWS:

Claims 1 - 15 (cancelled)

Claim 16. (Original) A method of forming CMOS devices featuring a channel region formed in a selectively grown, composite silicon layer, wherein said composite silicon layer is comprised of at least a strained SiGe layer and an overlying silicon layer, comprising the steps of:

providing a first region of said semiconductor substrate to be used as an NMOS region, and providing a second region of said semiconductor substrate to be used as a PMOS region;

forming shallow trench isolation (STI) regions in top portions of said semiconductor substrate, with a top portion of each STI region featuring tapered sides;

forming a P well region in a top portion of said NMOS region, and forming an N well region in a top portion of said PMOS region;

selectively depositing a composite silicon layer on the top surface of said P well region and on the top surface of said N well region, with said composite silicon layer featuring tapered sides, resulting in V-groove openings located between said tapered sides of said STI regions and tapered sides of said composite silicon layer, and with said composite silicon layer comprised of a silicon layer, a strained SiGe layer, and an overlying silicon layer;

depositing an insulator layer;

removing portion of insulator layer from the top surface of said composite insulator layer resulting in insulator filled V-grooves located between said STI regions and said composite silicon layer; and

thermally oxidizing a top portion of said overlying silicon layer to form a silicon dioxide gate insulator layer on a bottom portion of said overlying silicon layer.

Claim 17. (Original) The method of claim 16, wherein said STI regions are silicon oxide filled shallow trench shapes, formed to a depth between about 3000 to 6000 Angstroms in said semiconductor substrate.

Claim 18. (Original) The method of claim 16, wherein said composite silicon layer is obtained via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures, at a temperature between about 400 to 800° C, and at a pressure less than 200 mtorr.

Claim 19. (Original) The method of claim 16, wherein said SiGe layer is grown on an underlying silicon layer.

Claim 20. (Original) The method of claim 16, wherein said silicon layer of said composite silicon layer, underlying said SiGe layer, is selectively grown to a thickness between about 0 to 100 Angstroms, using silane or disilane as a source.

Claim 21. (Original) The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown to a thickness between about 20 to 150 Angstroms.

Claim 22. (Original) The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown with a germanium content between about 20 to 40 weight percent.

Claim 23. (Original) The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown using silane or disilane, and germane as reactants.

Claim 24. (Original) The method of claim 16, wherein said overlying silicon layer of said composite silicon layer, is selectively grown to a thickness between about 5 to 100 Angstroms using silane or disilane as a source.

Claim 25. (Original) The method of claim 16, wherein said insulator layer, used to fill said V-groove openings, is a silicon oxide layer, obtained via deposition of a silicon oxide at a thickness between about 100 to 1000 Angstroms.

Claim 26. (Original) The method of claim 16, wherein removal of said insulator layer used to form said insulator filled V- grooves, is accomplished via reactive ion etching procedures.

Claim 27. (Original) The method of claim 16, wherein said silicon dioxide gate insulator layer is obtained at a thickness between about 5 to 80 Angstroms, via thermal oxidation procedures performed at a temperature between about 600 to 900° C, in an oxygen - steam ambient.